PVP 14

Code: IT3T1

II B.Tech - I Semester–Regular/Supplementary Examinations
November 2018

DIGITAL SYSTEM DESIGN
(INFORMATION TECHNOLOGY)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) $(231.23)_4$ = _____(base 10)

b) Perform $(15)_{10}$-$(28)_{10}$ using 2's complement representation.

c) Perform $(24)_{10}$-$(56)_{10}$ in BCD using 10's complement representation.

d) Solve the (A+B)(A'+C)(B+C)(A'+D)(B+D) using Boolean Algebra.

e) Implement OR gate using NAND gates.

f) Express function (xy+z)(y+xz) in sum of minterms and product of maxterms

g) Define fan out of a logic gate.

h) What are the applications of shift register?

i) Compare a decoder with a Demultiplexer.

j) Show characteristic equation of JK-FF.

k) List basic types of programmable logic devices.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.
3 x 16 = 48 M

2. a) Explain about signed magnitude and 2's complement approaches for representing the fixed Point numbers. Why 2's complement is preferable? 4 M

b) The binary numbers listed have a sign bit in the left most position and, if negative, are in 1's complement form. Perform the arithmetic operations indicated and verify the answers. 12 M

i) 100101 + 110010

ii) 001000 + 101010

iii) 110011 - 001011

iv) 100001 – 110100

3. a) State and prove DeMorgan's laws. 8 M

b) Simplify the following Boolean expressions. 8 M

i) A'C'+ABC+AC' to three literals.

ii) (x'y'+z)'+z+xy+wz to three literals.

iii) A'B(D'+C'D)+B(A+A'CD) to one literal.

iv) (A'+C)(A'+C')(A+B+C'D) to four literals.

4. a) Design an 8-bit BCD adder using 4-bit binary adder. 8 M

b) Design a full - subtractor circuit with three inputs x,y,z and outputs D, B. The circuit subtracts X - Y - Z where Z is the input borrow, B is the output borrow and D is the Difference draw the circuit using NAND gates. 8 M

5. List the PLA programming table and draw the PLA structure for the BCD-to-Excess-3-code converter. 16 M

6. a) Design a BCD ripple counter using JK flip-flop. 12 M

b) What is SR latch? Explain its operations. 4 M